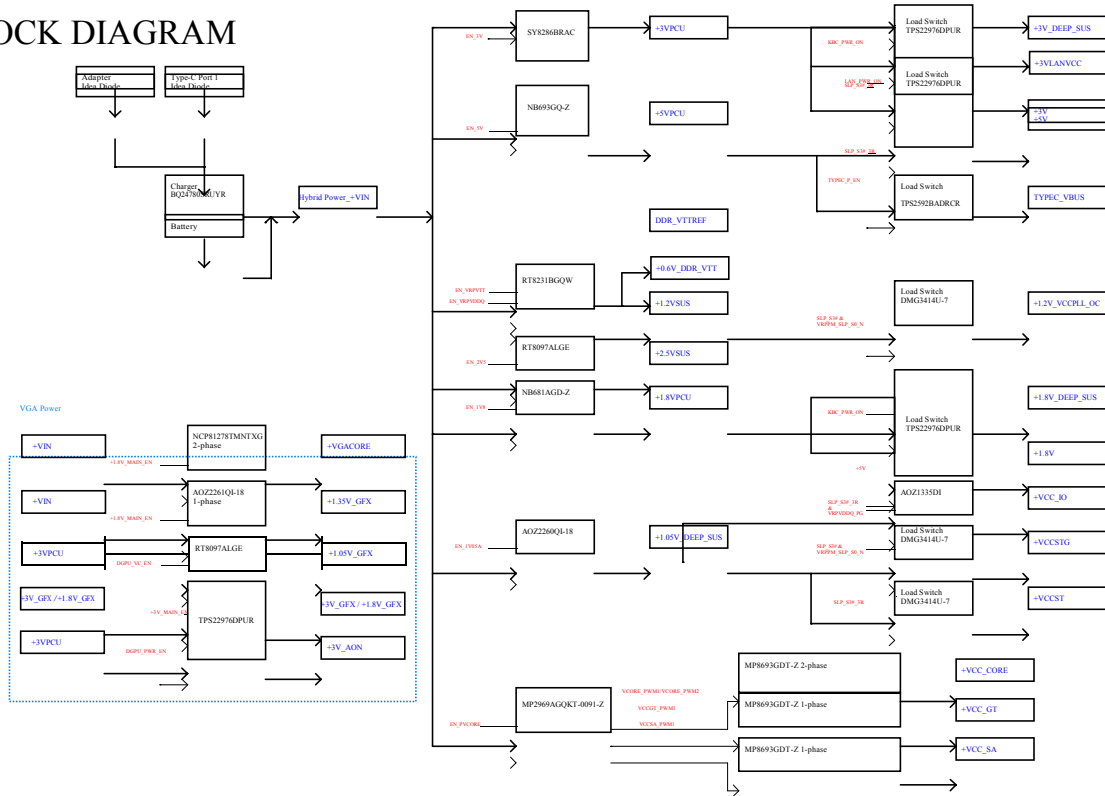
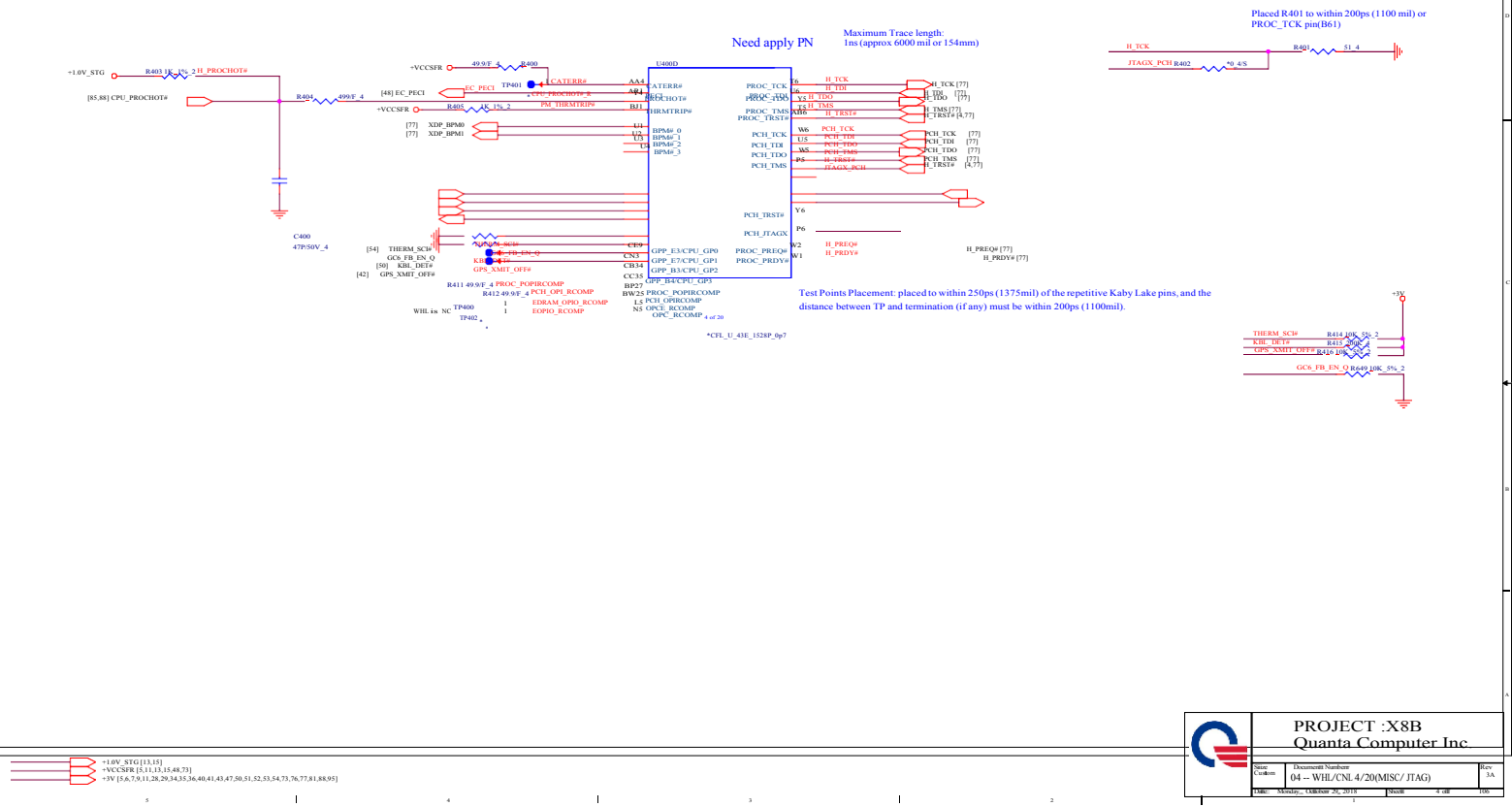
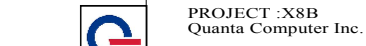
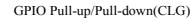
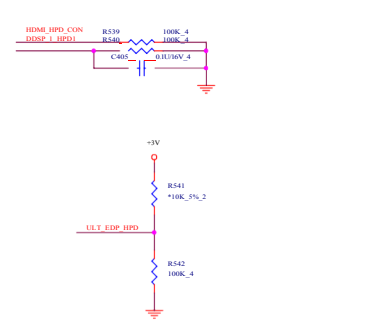
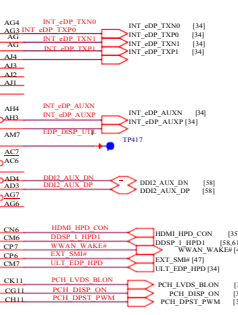
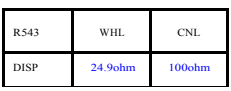
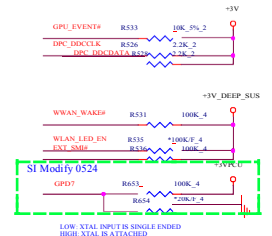
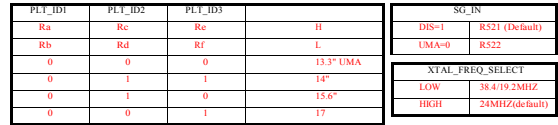


POWER BLOCK DIAGRAM



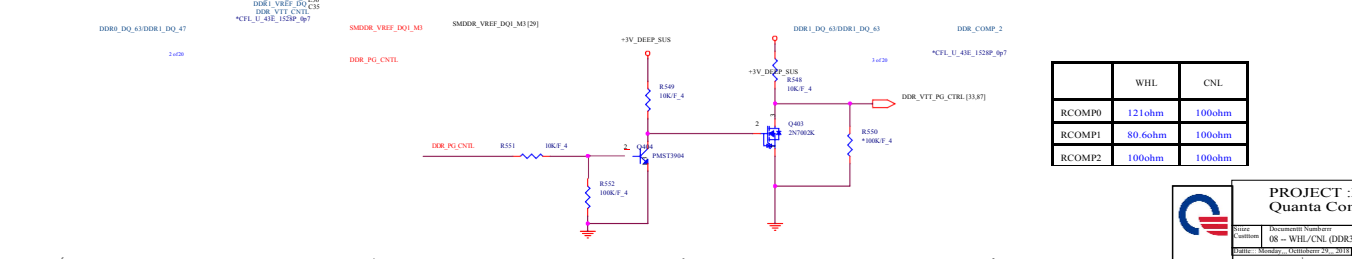
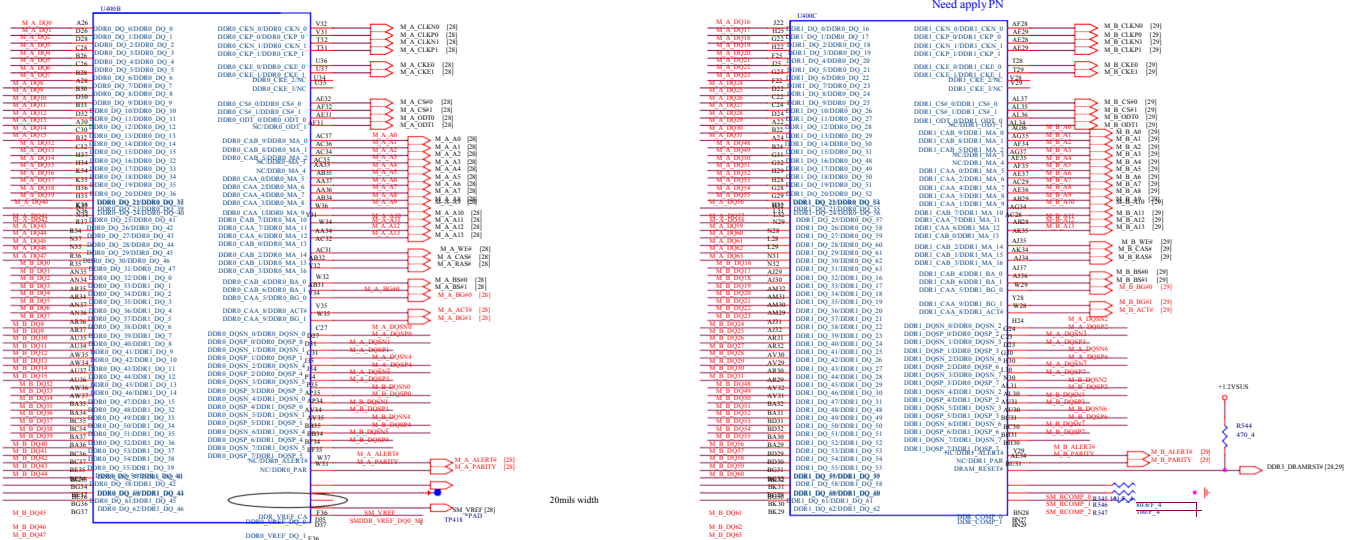






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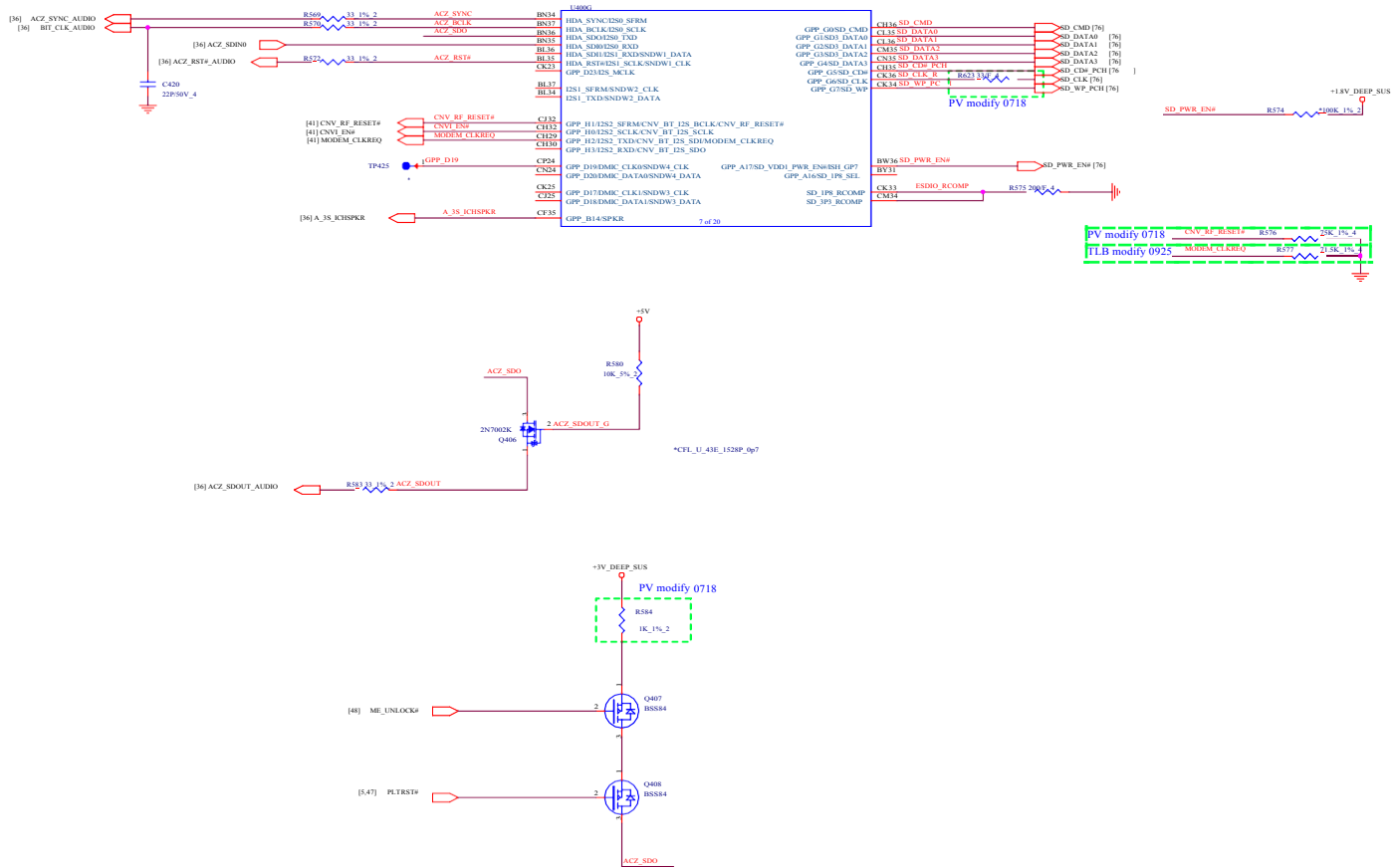
Need apply PN



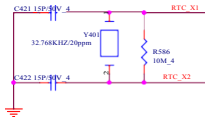
	WHL	CNL
RCOMP1	121ohm	100ohm
RCOMP2	80.6ohm	100ohm
RCOMP3	100ohm	100ohm

PROJECT :X8B
Quanta Computer Inc.

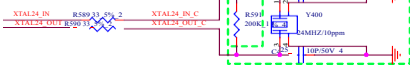
Customer: Dell
 Document Number: 08 - WHL/CNL (DDR3-A/B/F)
 Revision: 1.0
 Date: 2013/08/14



RTC Clock 32.768KHz



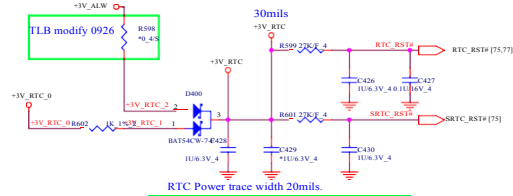
PV Modify 0727



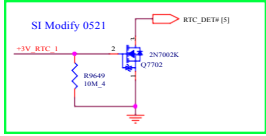
SI Modify 0521



RTC Circuitry(RTC)

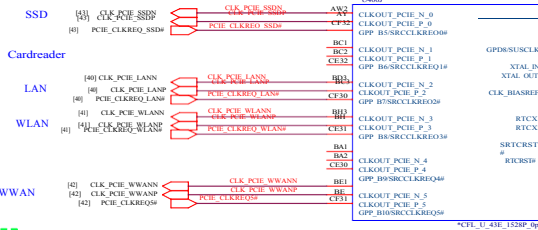


RTC Power trace width 20mils.

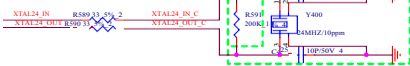


CFG1 R605 1K 1% 2

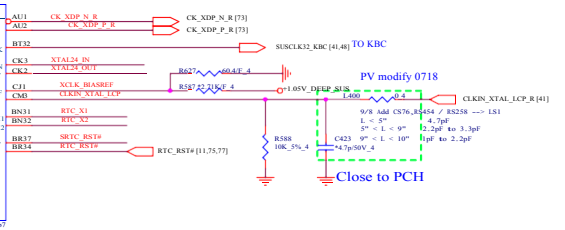
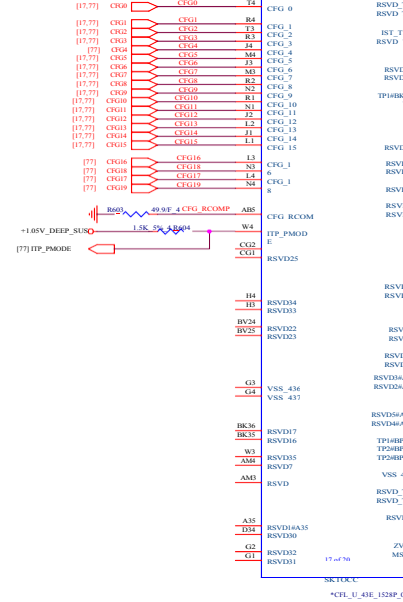
+VCCSR [45,13,15,48,73]
+1.8V_DEEP_SUS [12,73,77,92,96]
+3V [4,5,6,7,9,24,29,34,35,36,40,41,43,47,50,51,52,53,54,73,76,77,81,88,95]



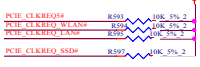
SI Modify 0530



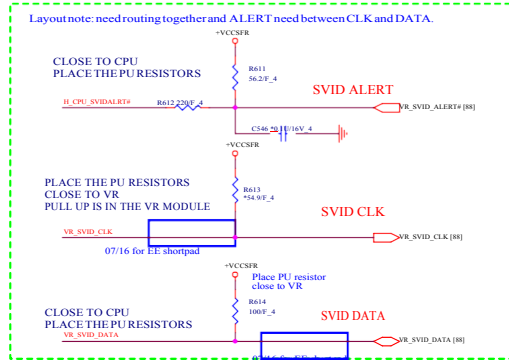
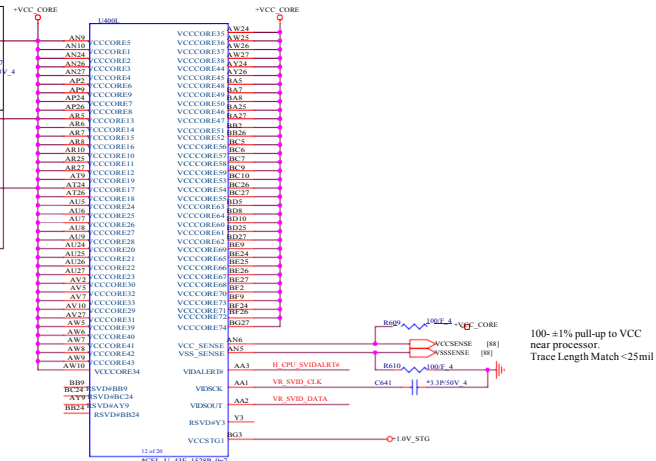
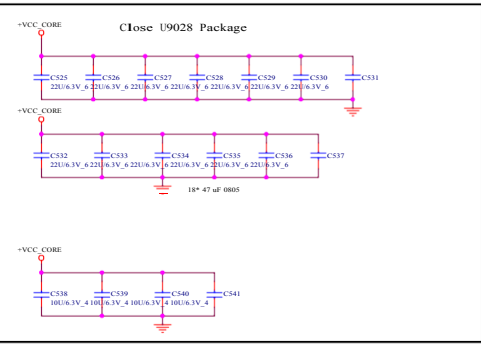
CFG0-19 need Reserve TP



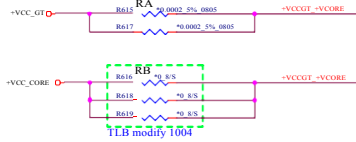
CLK_REQ/Strap Pin(CLG)



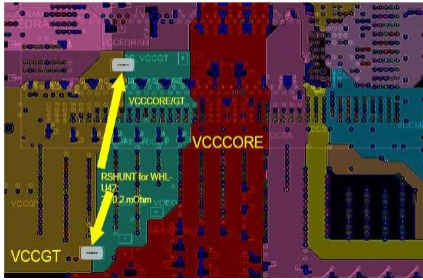
PROJECT :X8B Quanta Computer Inc.		Rev 1A
Doc 11 -- WHL/CNL (CLK/RSV/RTC)	Doc Monday, October 20, 2015	Doc 11:08



	WHL-U42f ES1 CNL-U22	WHL-U42 ES2
RA	STUFF	NI
RB	NI	STUFF

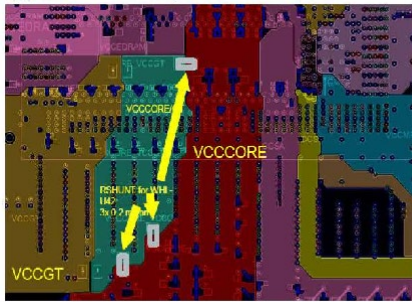


Routing guideline for RSHUNT placement for WHL ES1, CFL43e and CNLU22

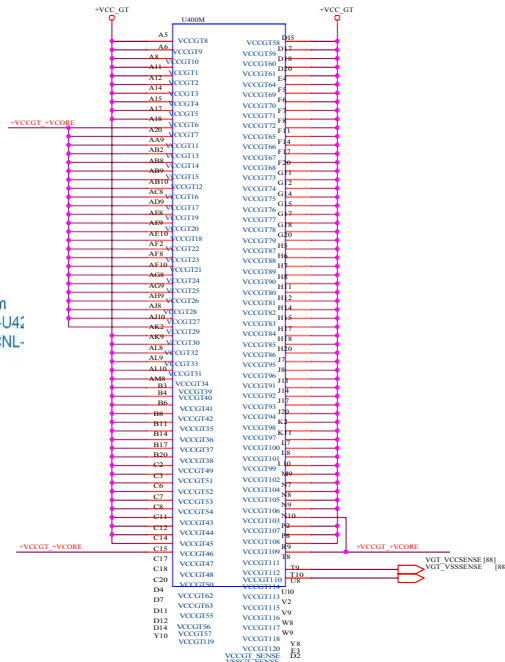


Place 2x 0.2 mOhm
RSHUNT for WHL-U4;
(ES1)/CFL-U43e/CNL-
U22

Routing guideline for RSHUNT placement for WHL ES2

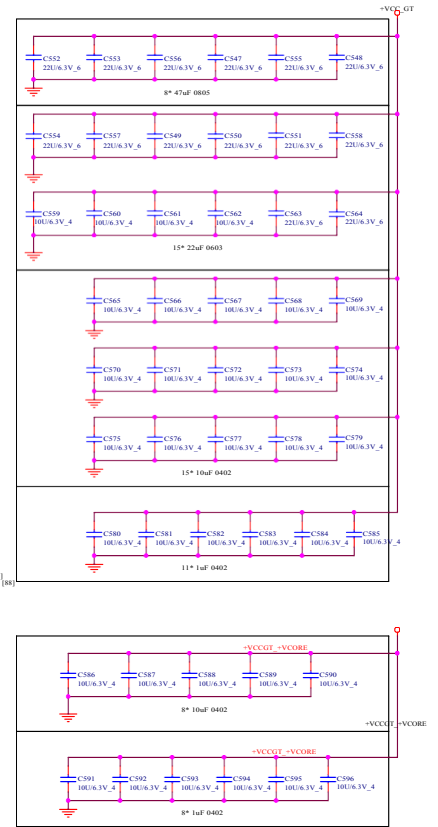


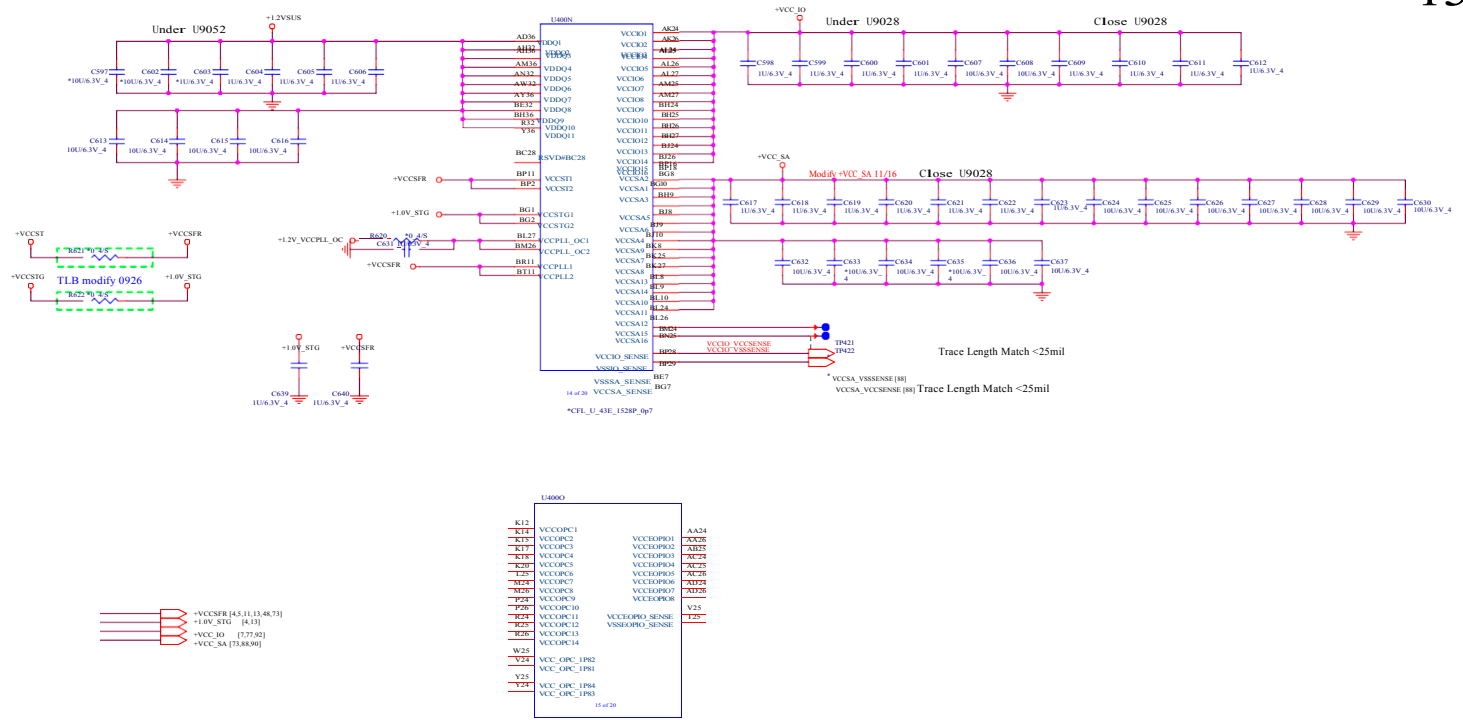
Place 3x 0.2 mOhm
RSHUNT for WHL-
U42 (ES2)



Trace Length Match <25mil

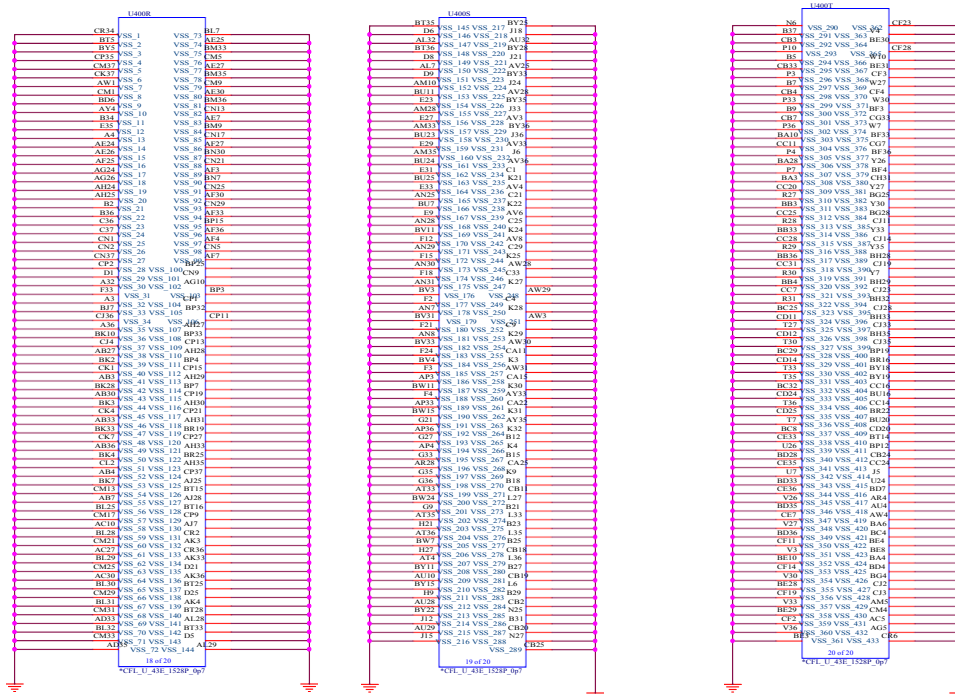
*CFL_U_43e_1520P_dp7

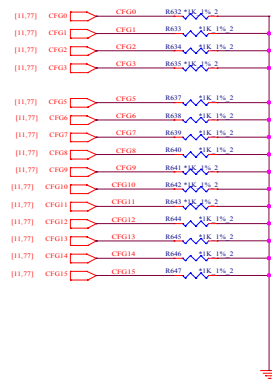




*CPL_U_43E_1528P_0p7

		PROJECT :X8B	
		Quanta Computer Inc.	
Rev	15 -- WHL/CNI (POWER-3)	Rev	15
Date	2018.08.20	Sheet	106





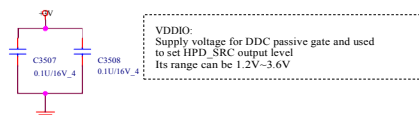
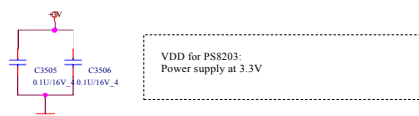
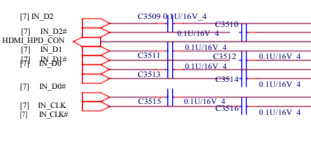
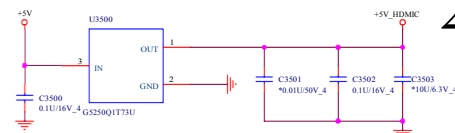
EMI Solution

TX2_HDMI-	R3506	*150 5% 4	TX2_HDMI-
TX1_HDMI-	R3507	*150 5% 4	TX1_HDMI-
TX0_HDMI-	R3508	*150 5% 4	TX0_HDMI-
TXC_HDMI-	R3509	*150 5% 4	TXC_HDMI-

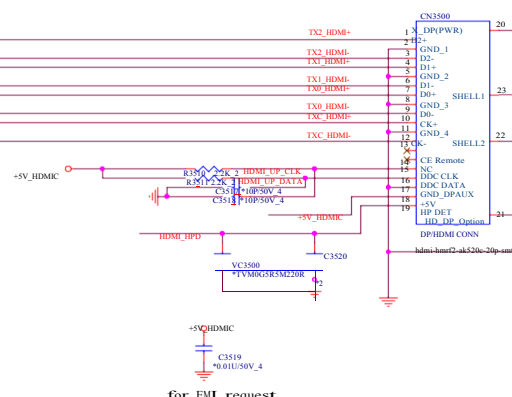
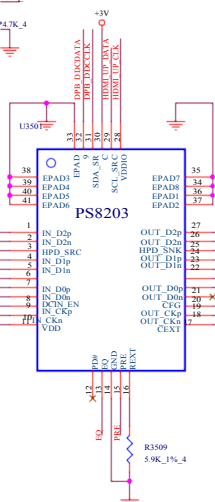
Output pre-emphasis setting; Internal pull down at ~150k Ω , 3.3V
 L: no pre-emphasis
 H: 2.5dB pre-emphasis

Receiver equalization setting; Internal pull down at ~150k Ω , 3.3V
 L: programmable EQ for channel loss up to 12.4dB @ 30bps
 H: programmable EQ for channel loss up to 4.5dB @ 30bps
 V: programmable EQ for channel loss up to 8.6dB @ 30bps

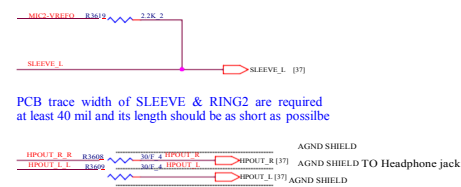
EQ coupling enable; Internal pull down at ~150k Ω , 3.3V
 L: default, AC coupling input
 H: DC coupling input



HDMI SMBus Isolation



for EMI request



Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

Close to Speaker

1.366022 1 * 10⁻⁶ S
1.366022 1 * 10⁻⁶ S
1.366022 1 * 10⁻⁶ S
1.366022 1 * 10⁻⁶ S

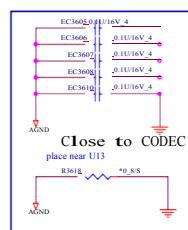
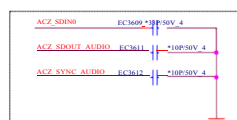
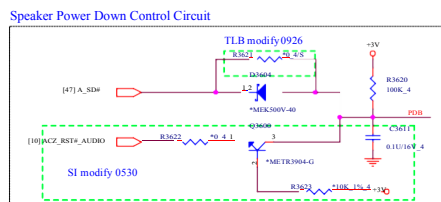
L+SPK+
R+SPK+
C+SPK+

1.366022 1 * 10⁻⁶ S
1.366022 1 * 10⁻⁶ S
1.366022 1 * 10⁻⁶ S
1.366022 1 * 10⁻⁶ S


L+SPK+
R+SPK+
C+SPK+

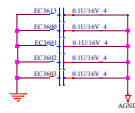
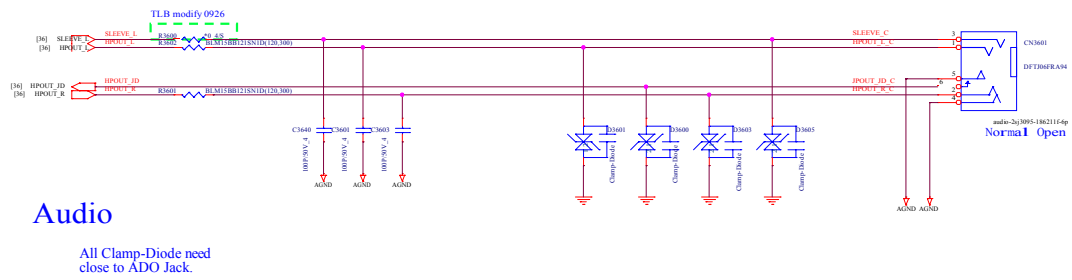
C3635 1000P-50V_4
C3636 1000P-50V_4
C3637 1000P-50V_4
C3638 1000P-50V_4

CNS600
1 2 3 4
INT SPEAKER CONN

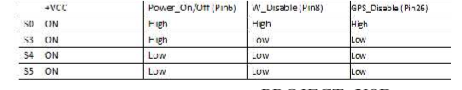
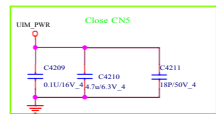
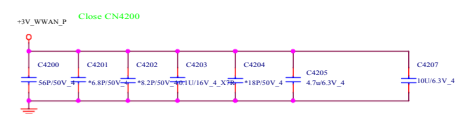
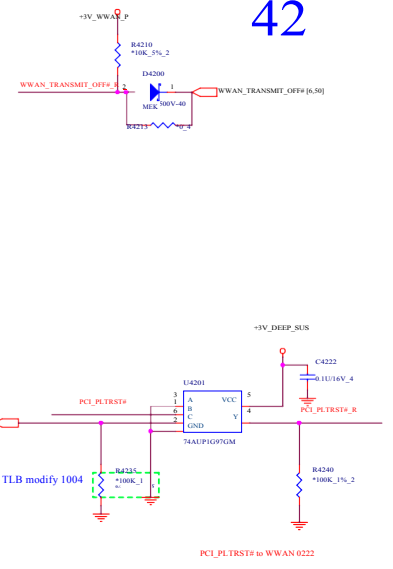


[7,9,81,95] +1.8V
[4,5,6,7,9,11,28,29,34,35,40,41,43,47,50,51,52,53,54,73,76,77,81,88,95] +3V
[10,34,35,44,50,54,61,73,81,95] +5V

	PROJECT :X8B Quanta Computer Inc.		
	Source Location 36 -- Audio Codec CX7501	Document# Numbr 36 -- Audio Codec CX7501	Rev 3A
Date-Msg: 07/05/99 20:18	Sheet 36 of 110	1/10	

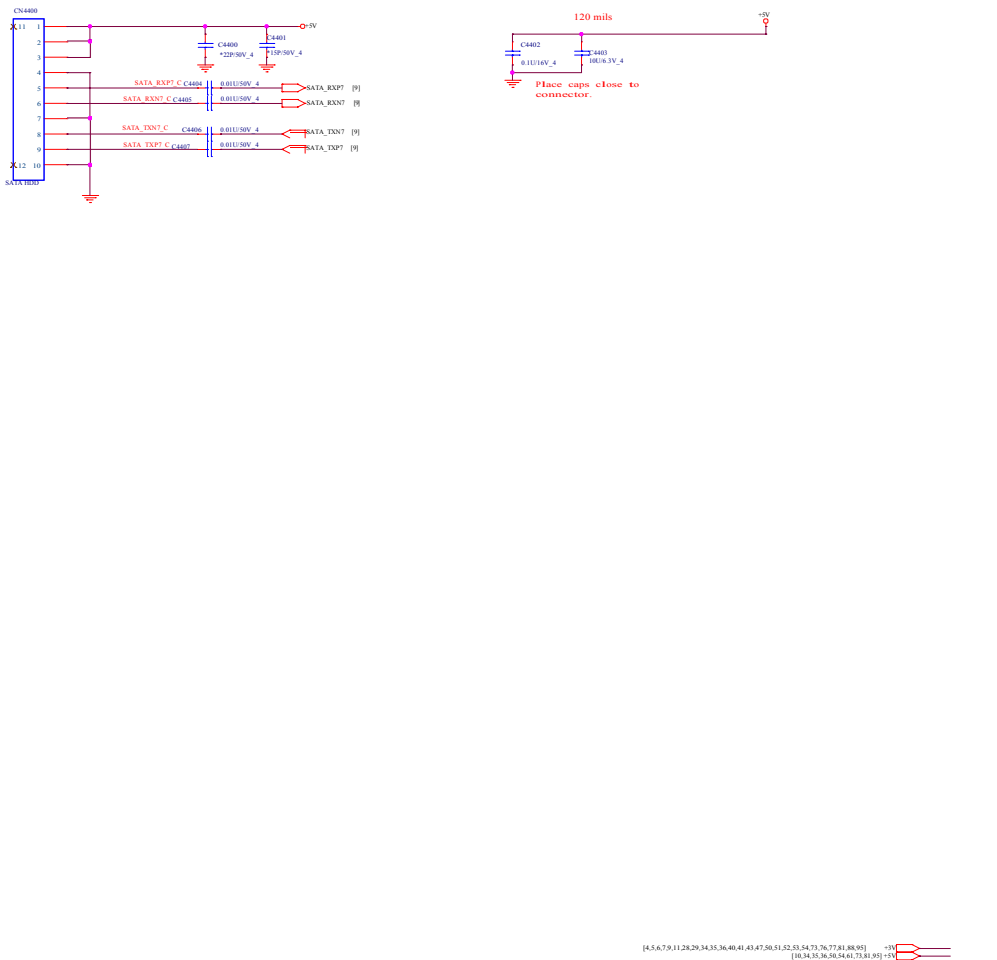






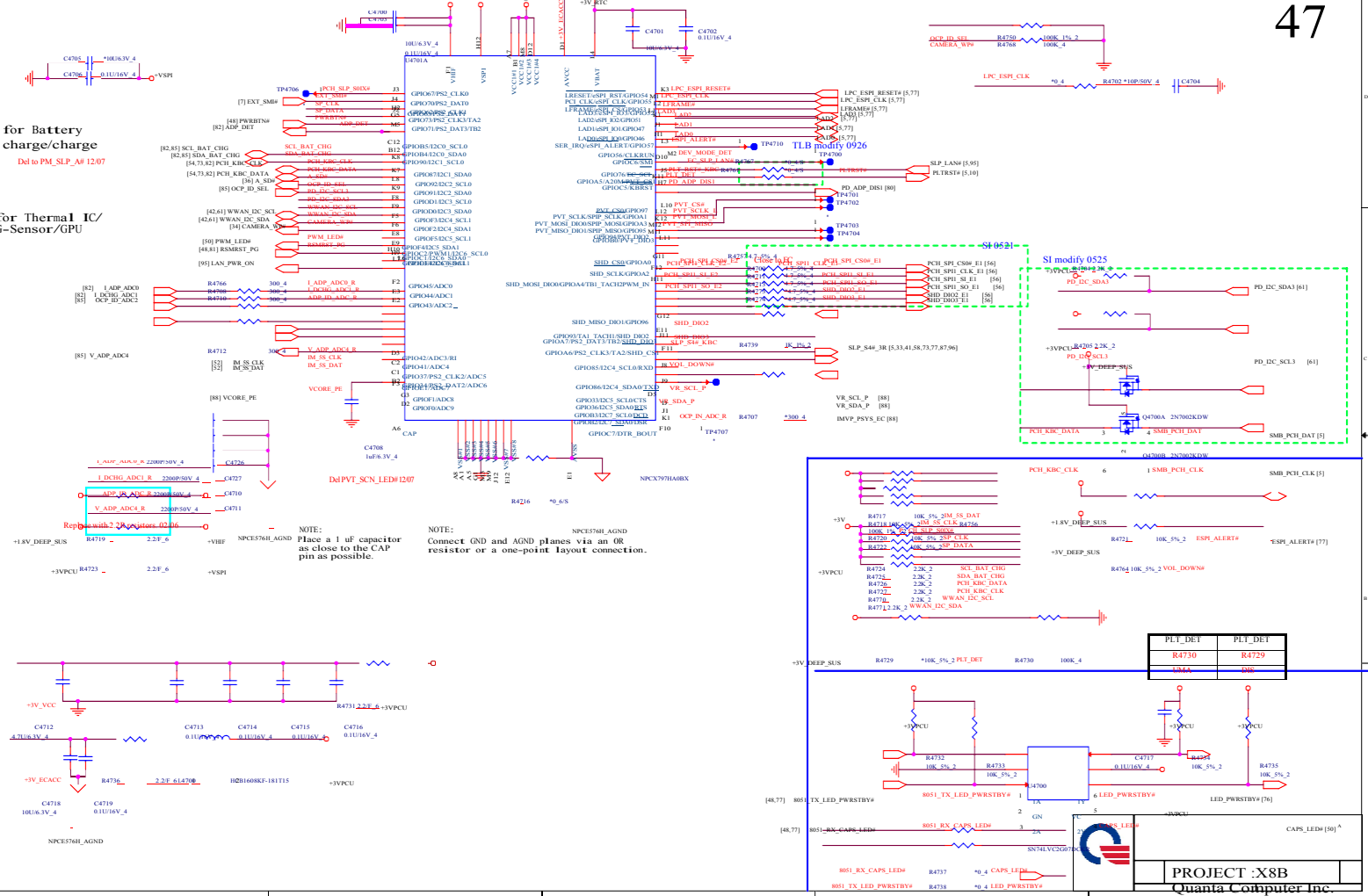
+VCC		Power_On/Off (Pink)	W_Disable (Pink)	GPS_Disable (Pink)
S0	ON	High	High	High
S3	ON	High	Low	Low
S4	ON	Low	Low	Low
S5	ON	Low	Low	Low

SATA-HDD



for Battery
charge/charge
Del to PM_SLP_A# 1207

for Thermal IC/
6-Sensor/GPU

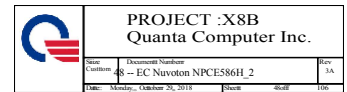


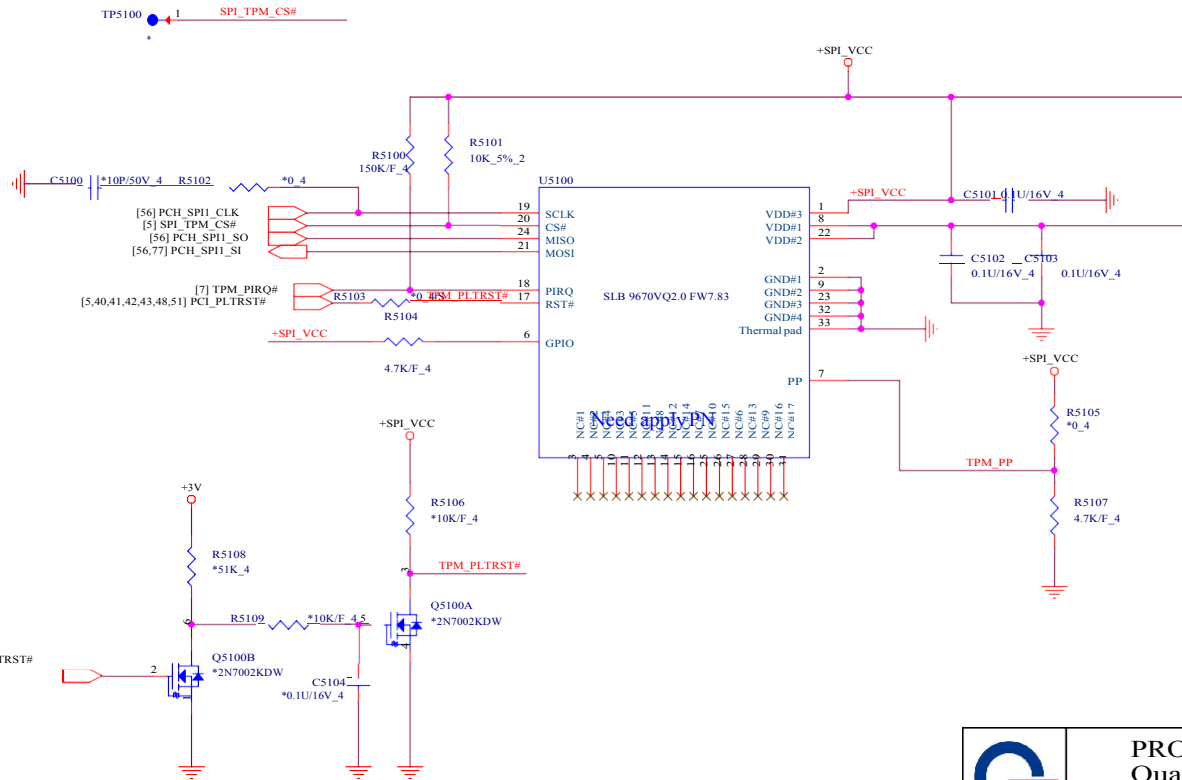
[43,6,7,9,11,28,29,34,35,36,40,41,43,50,51,52,53,54,73,76,77,81,88,95]


+1V

Sheet Documents Number
47-EC Navon NPCE586H_1
Date: Monday, October 29, 2018
Sheet 34 of 106

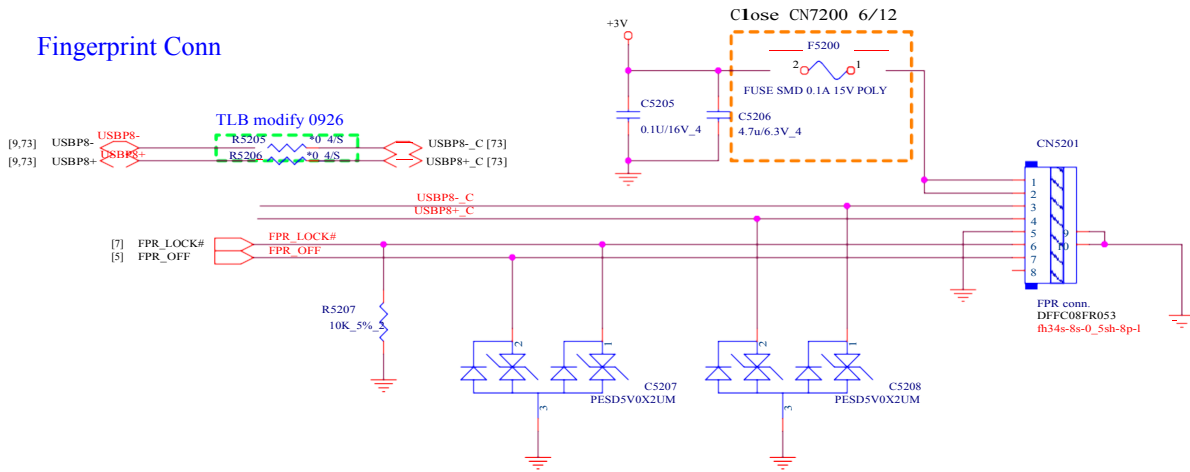
4



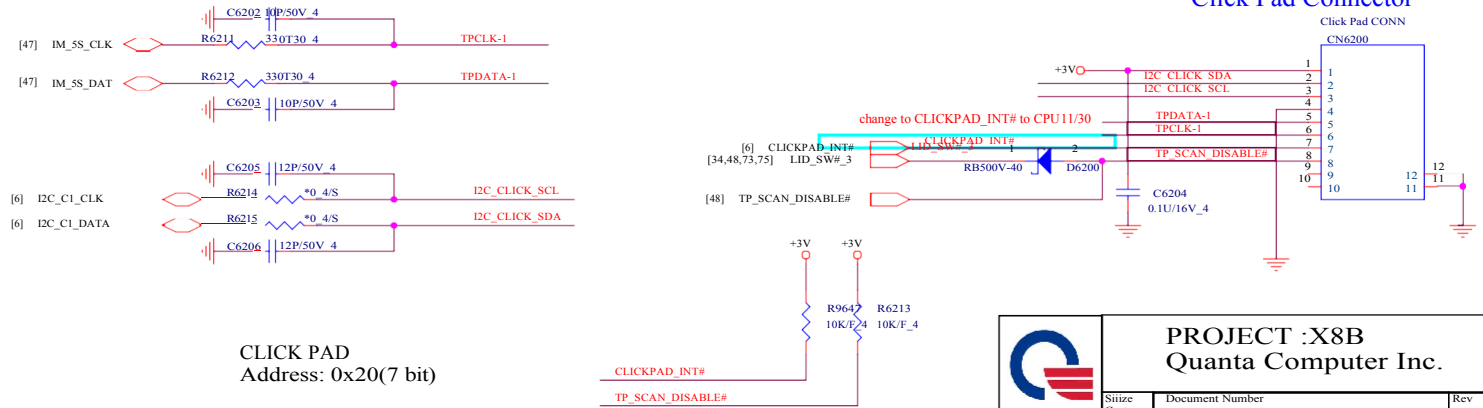


 PROJECT :X8B Quanta Computer Inc.		
Site Custom	Document Number 51 -- TPM SLB9670_QFN	Rev .3A
Date: Monday, October 29, 2018	Sheet 51 of 106	

Fingerprint Conn



Click Pad Connector



CLICK PAD
Address: 0x20(7 bit)

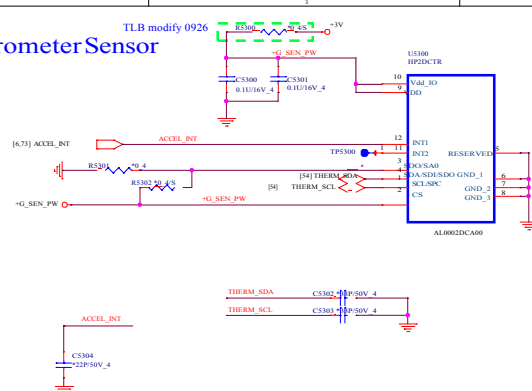
CLICKPAD_INT#
TP_SCAN_DISABLE#



PROJECT :X8B
Quanta Computer Inc.

Site	Document Number	Rev
Custom	52 -- FPR / Click PAD	3A
Date: Monday, October 29, 2018	Sheet 52 of 106	

Accelerometer Sensor



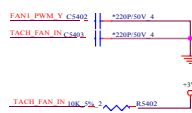
[4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,54,73,76,77,81,88,95] +3V

[5,7,12,33,34,36,41,42,47,48,50,54,58,61,73,75,77,80,81,82,85,86,87,88,92,93,95] +1VPCU

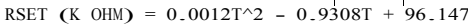


PROJECT :X8B
Quanta Computer Inc.

State Custom	Document Number 53 -- TS and Accelerometer	Rev 3A
-----------------	---	-----------



1

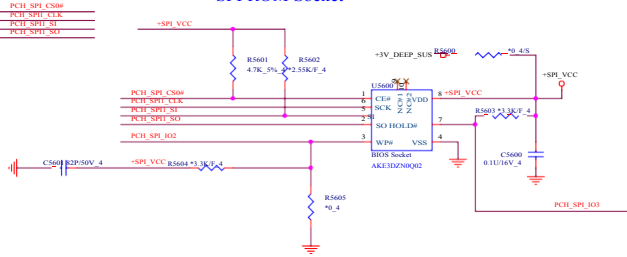


Over Temperature Protection		
DEGREE	R5406	
68	38.4K	CS33832FB08
70	36.5K	
73	34K	CS33402FB18
75	33.2K	CS33322FB13
81	28K	
85	25.5K	CS32552FB11

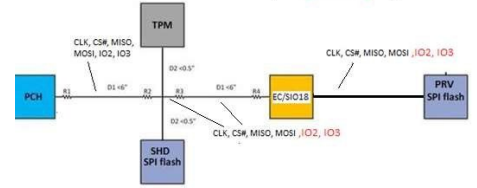
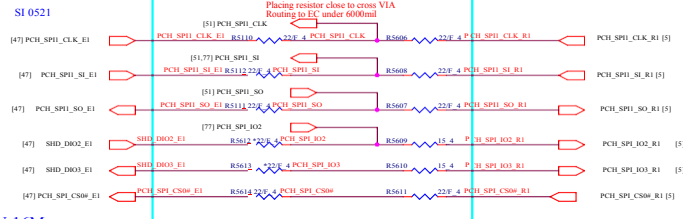
[4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,73,76,77,81,88,95] +3V
[11,33,41,73,75,81,85,86,87,93] +3V_ALW

Vendor	Size	P/N
GD	128MB	AKE2DF00Q00 Pilot run stage
Winbond	128MB	AKE3DF-KN00
Socket		DFHS08FS046
GD	128MB	AKE3DZN0Q02 MV stage
Winbond	128MB	AKE3DF-KN01

PCH SPI ROM(CLG)
Place TP at TOP side



PCH 6*5mm WSON 16M
SPI ROM Socket



Based on EC18 testing: PCH to TPM/SPI flash = Quad I/O, SIO18 to SPI Flash = Dual I/O Quad I/O,
R1=4.7 ohm for CLK, CS#, MISO, MOSI; R1 = 0 ohm for IO2, IO3
R2=22 ohm for CLK, CS#, MISO, MOSI; R2 = 15 ohm for IO2, IO3
R3=22 ohm for CLK, CS#, MISO, MOSI; R3 = for IO2, IO3 22 ohm
R4=4.7 ohm for CLK, CS#, MISO, MOSI; R4 = for IO2, IO3 4.7 ohm
Use same values to start on IO2 and IO3
Note: The value of the resistors should be tuned according to the signal integrity simulations or actual PCB measurements.

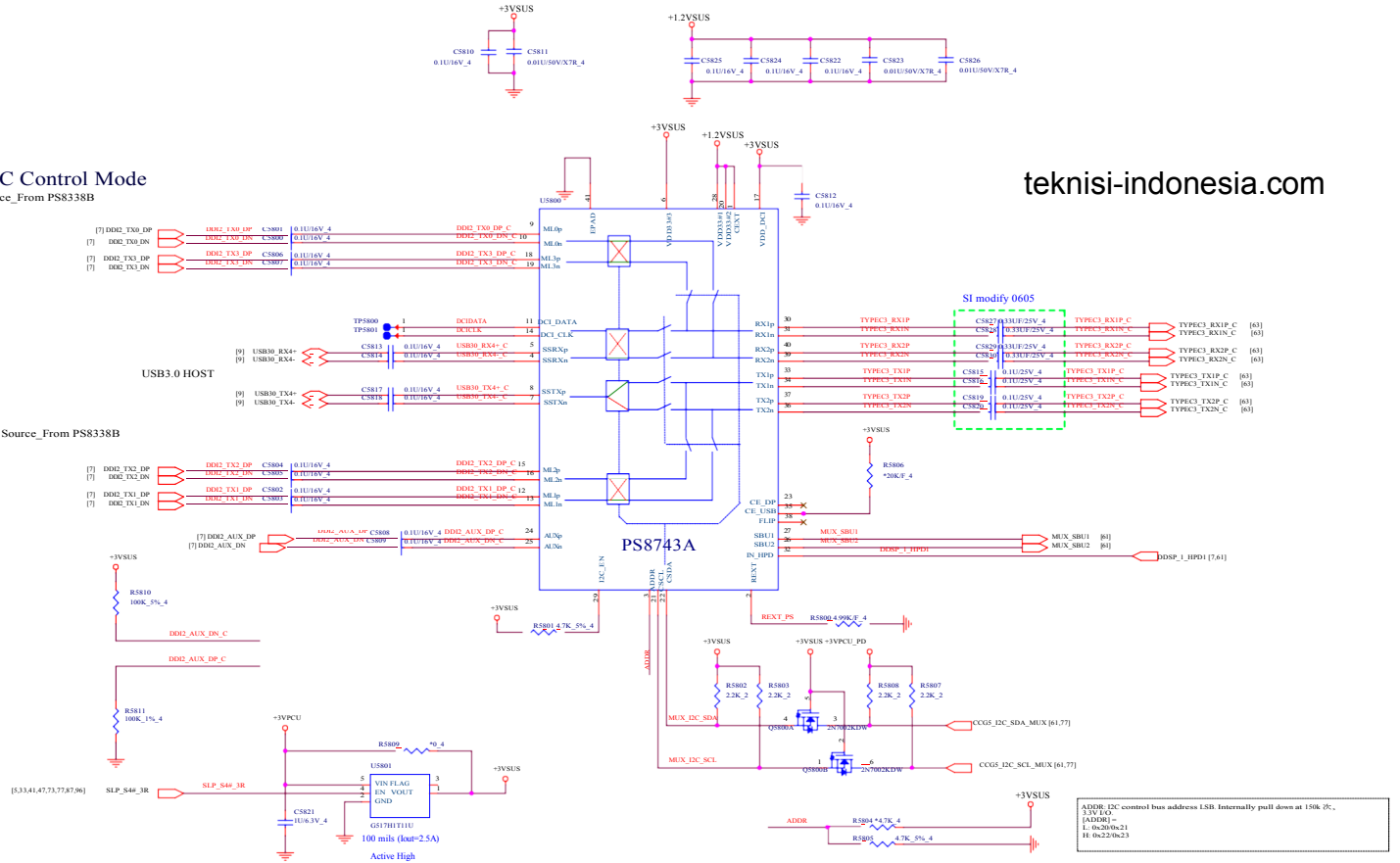
	PROJECT :X8B	
	Quanta Computer Inc.	
	<small>Sheet</small>	<small>Document Number</small>
<small>Custom</small>	S7-USB3.0 x2	<small>Rev</small>
<small>Drawn</small>	<small>Monday, October 29, 2018</small>	<small>Sheet 35 of 36</small>

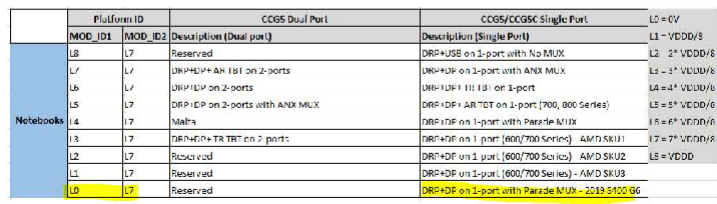
PS8743 I2C Control Mode

DisplayPort Source_From PS8338B

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DisplayPort Source_From PS8338B

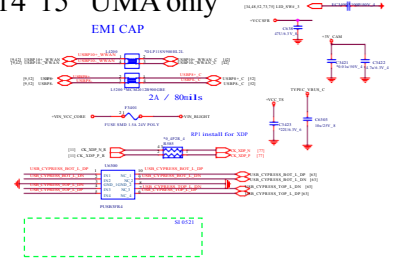




	Platform ID		CCGS Dual Port	CCGS/CCGS Single Port	L0 = EV
	MOD_ID1	MOD_ID2	Description (Dual port)	Description (Single Port)	L1 = VDDO/S
Notebooks	L8	L7	Reserved	DRP+USB on 1-port with No MUX	L2 = VDDO/S
	L7	L7	UN+V+P on 2-ports	UN+V+P on 1-port with ANX MUX	L3 = VDDO/S
	L6	L7	UN+V+P on 2-ports	DRP+L1P11111 or 1-port	L4 = VDDO/S
	L5	L7	DRP+P on 2-ports with ANX MUX	DRP+DP on 1-port on 1-port (700, 800 Series)	L5 = VDDO/S
	L4	L7	MUX	DRP+DP on 1-port with Parallel MUX	L6 = VDDO/S
	L3	L7	DRP+P+T+TR on 2 ports	DRP+DP on 1 port (600/700 Series)	L7 = VDDO/S
	L2	L7	Reserved	DRP+DP on 1 port (600/700 Series)	L8 = VDDO
	L1	L7	Reserved	DRP+DP on 1-port (600/700 Series)	
	L0	L7	Reserved	DRP+DP on 1-port with Parallel MUX	
	L0	L7	Reserved	DRP+DP on 1-port with Parallel MUX	

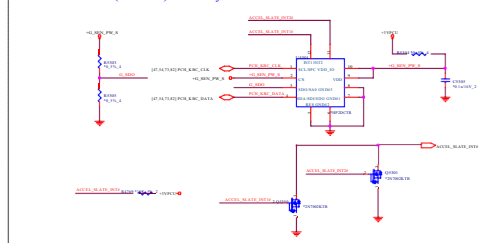
14"15" UMA only

EMI CAP

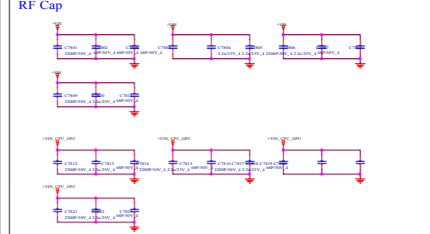


G-Sensor (SLATE) 360 only

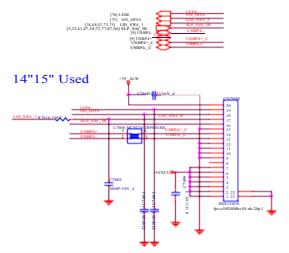
14"15" Used



RF Cap



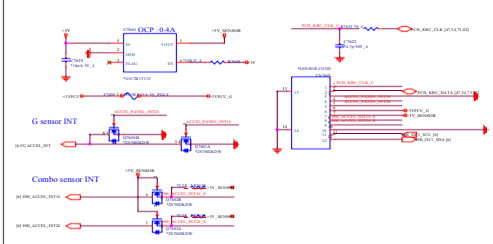
USB LID Daughter Board Connector



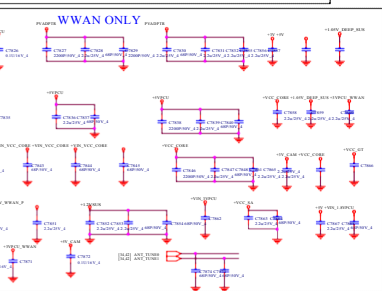
14"15" Used

Sensor connector for 360

14"15" Used



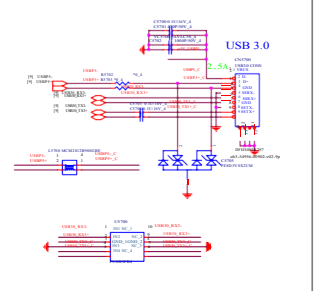
14 UMA RF Cap



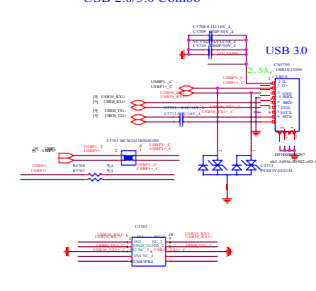
WWAN ONLY

USB 2.0/3.0 Combo

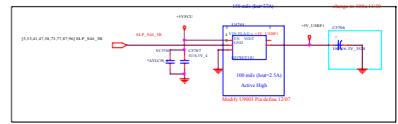
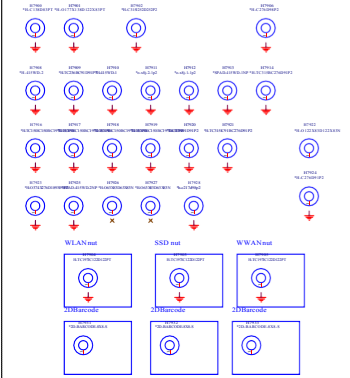
14"15" Used



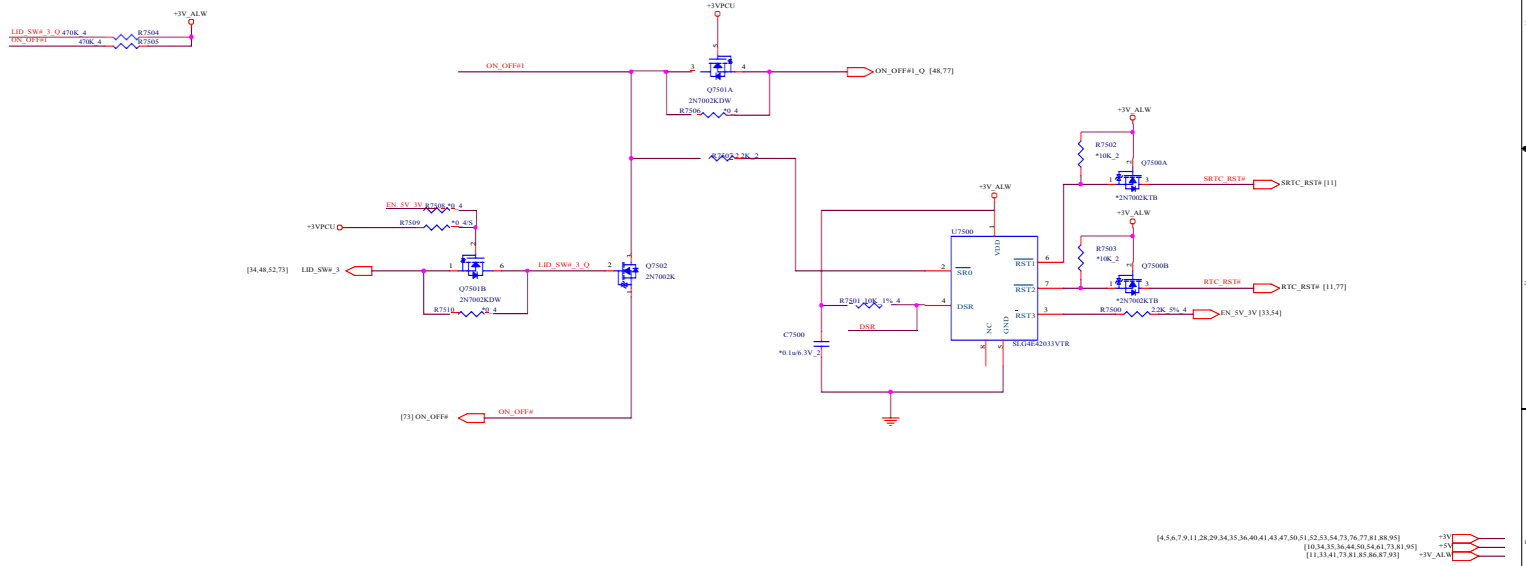
USB 2.0/3.0 Combo




14"15 Hole



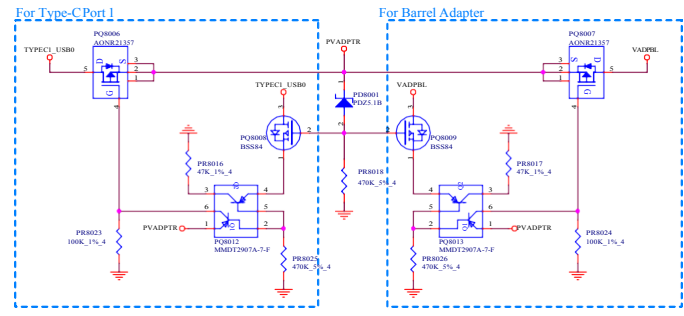
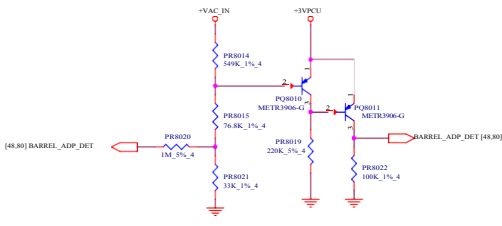
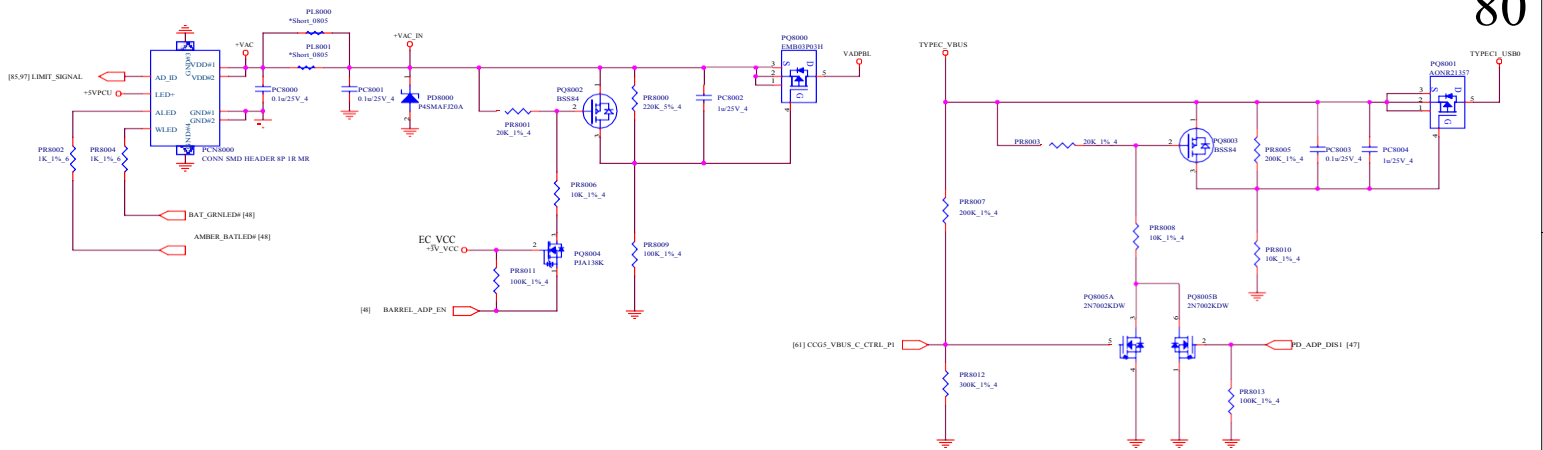
Power Button Connector



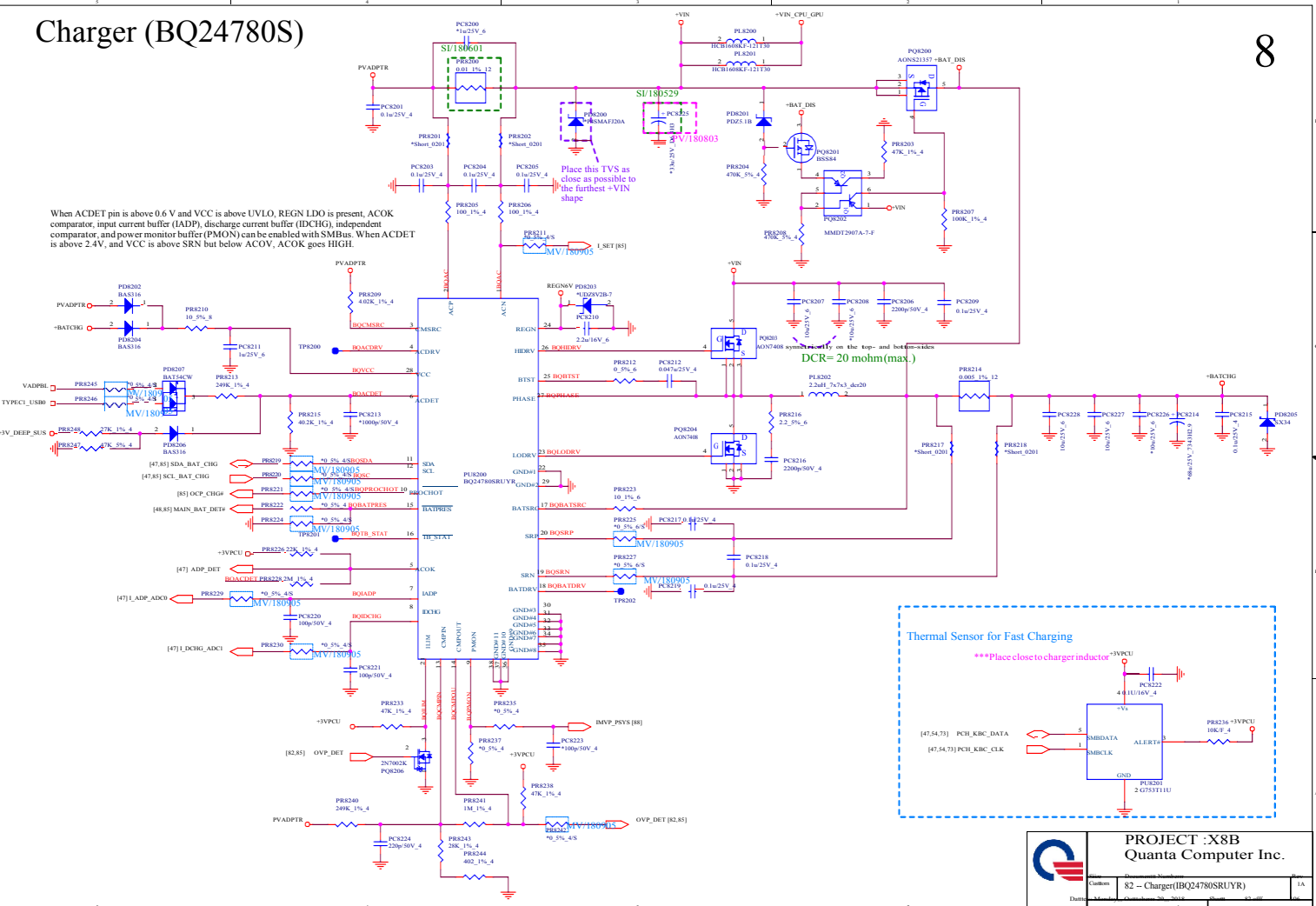



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Quanta Computer Inc.

Sheet	Document Number	Rev
Castform	25 -- LVDS converter RTD2136	3A
Date	Monday, October 29, 2018	16C




When ACDET pin is above 0.6 V and VCC is above UVLO, REGN LDO is present, ACOK comparator, input current buffer (IADP), discharge current buffer (DCHG), independent comparator, and power monitor buffer (PMON) can be enabled with SMBus. When ACDET is above 2.4V, and VCC is above SRN but below ACOV, ACOK goes HIGH.





PROJECT :X8B
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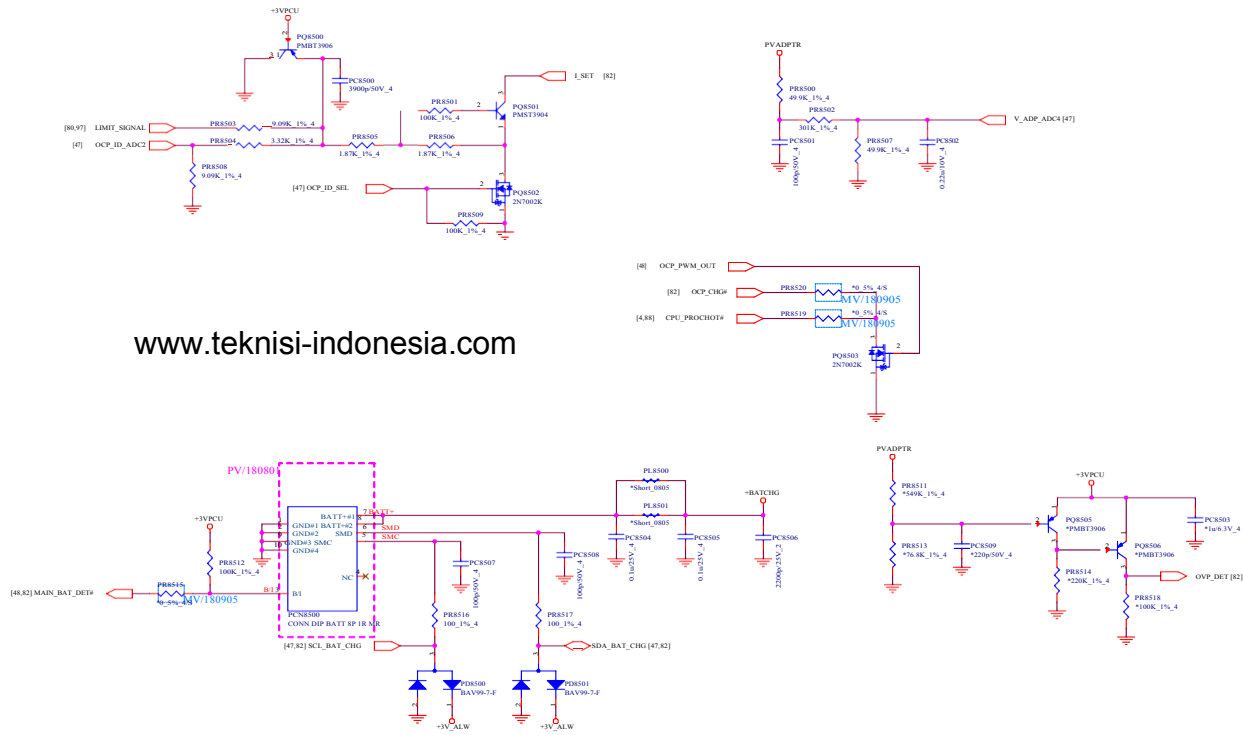
Sheet	Document Number	Rev
Custom	83 - Charger (ISL9538HRTZ-T)	1.0
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Custom	84 - Charger (ISL9538HRTZ-T)	1A
Drawn	Murphy, Christopher 29/ 2018	Sheet 84.dwg 06

Barrel Adapter OCP



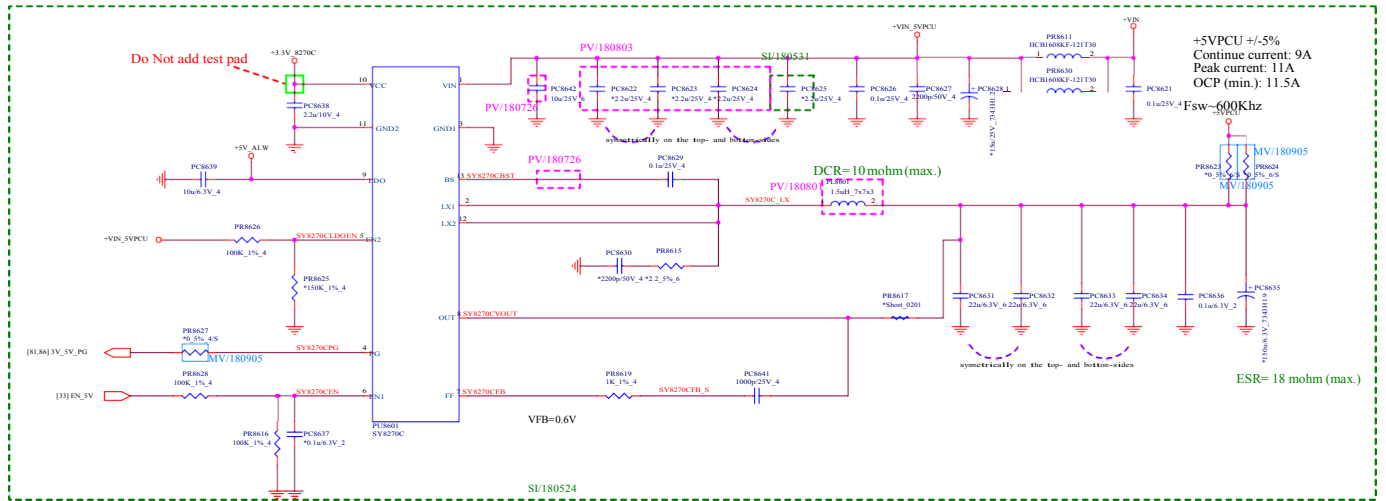
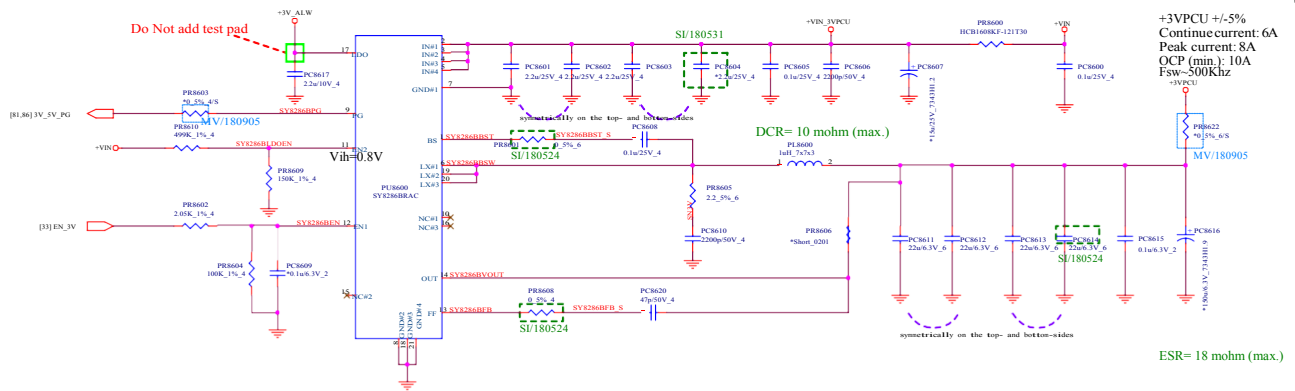
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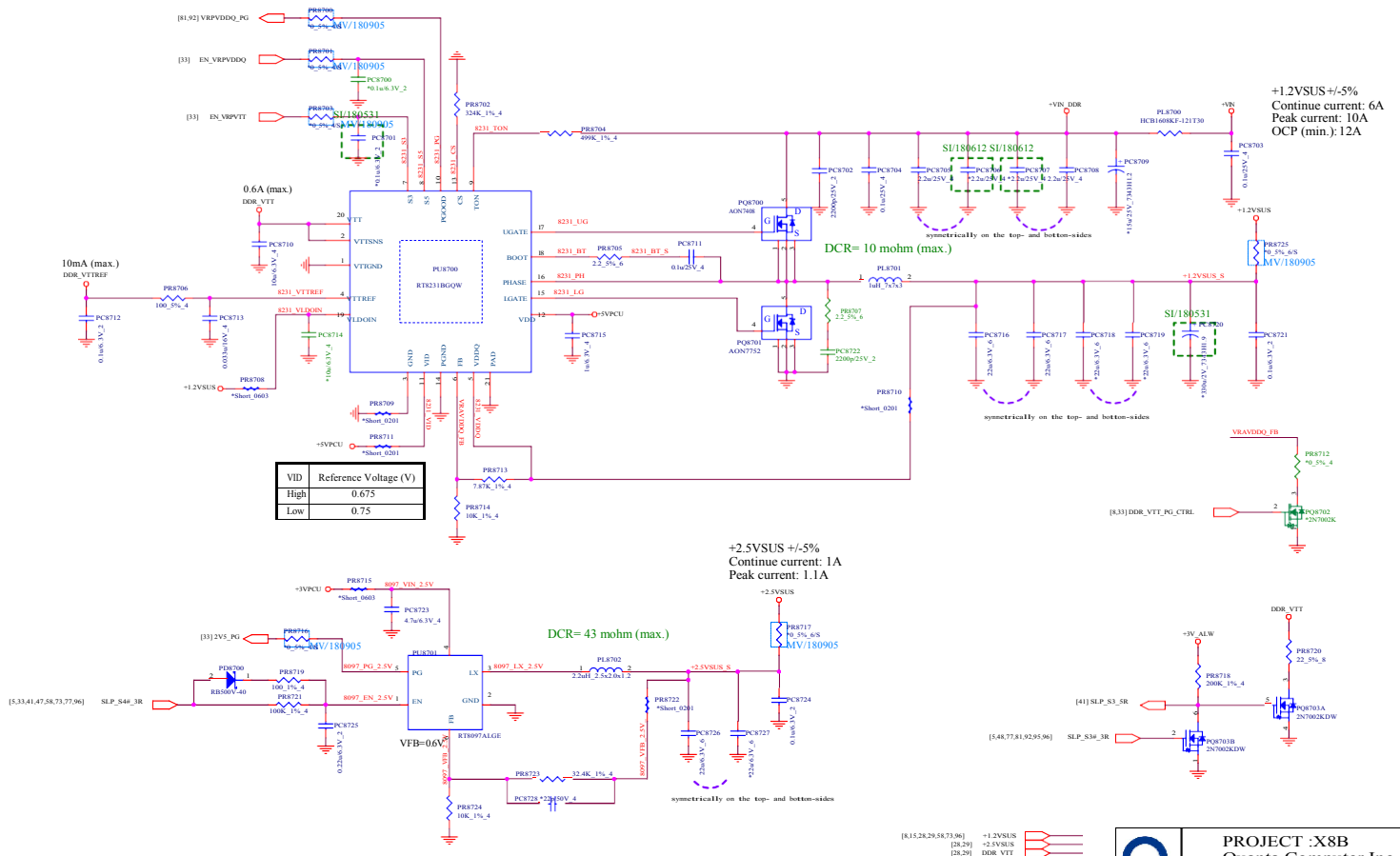


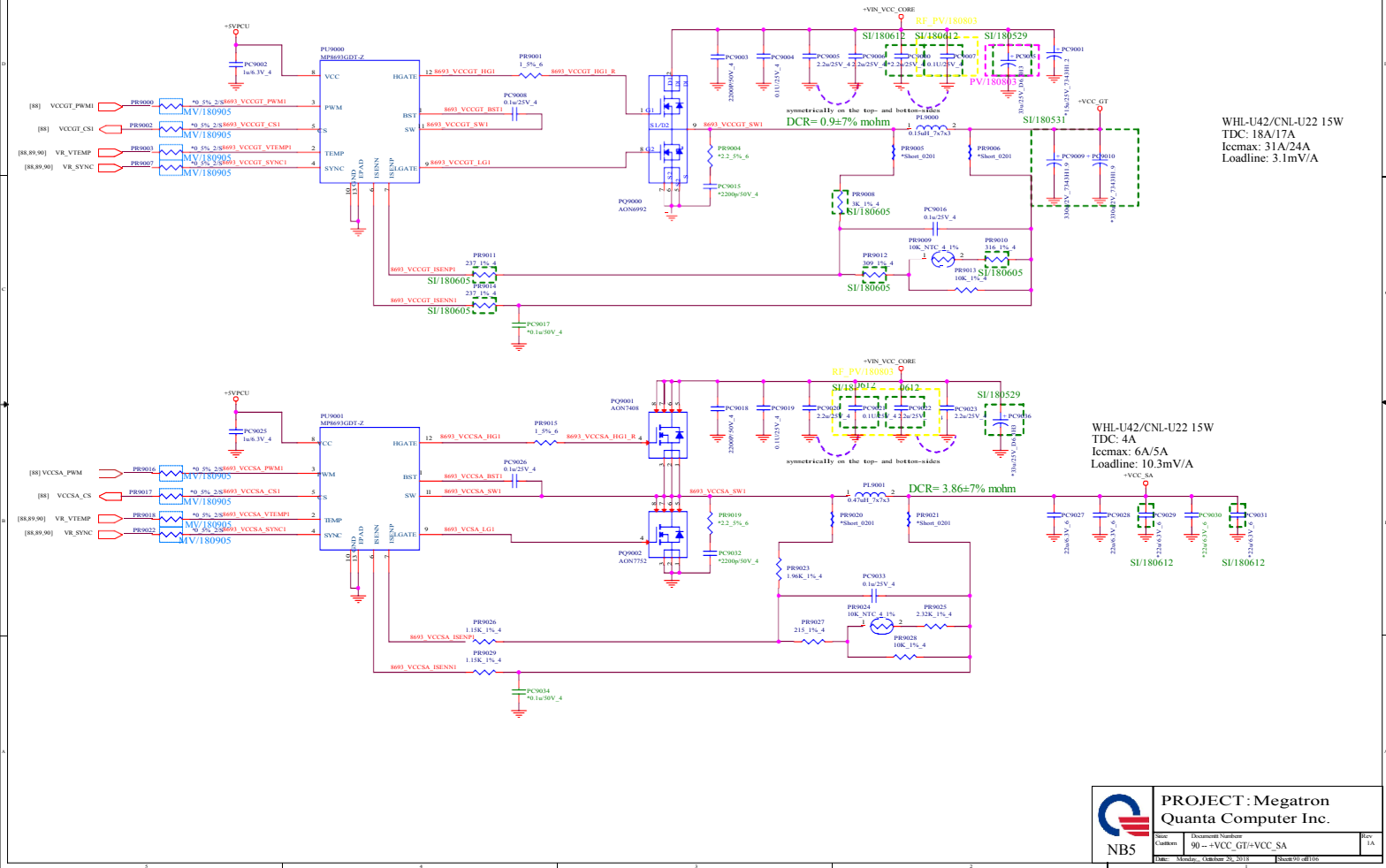
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State: California	Document# Number: 85 -- Charger	Rev 1A
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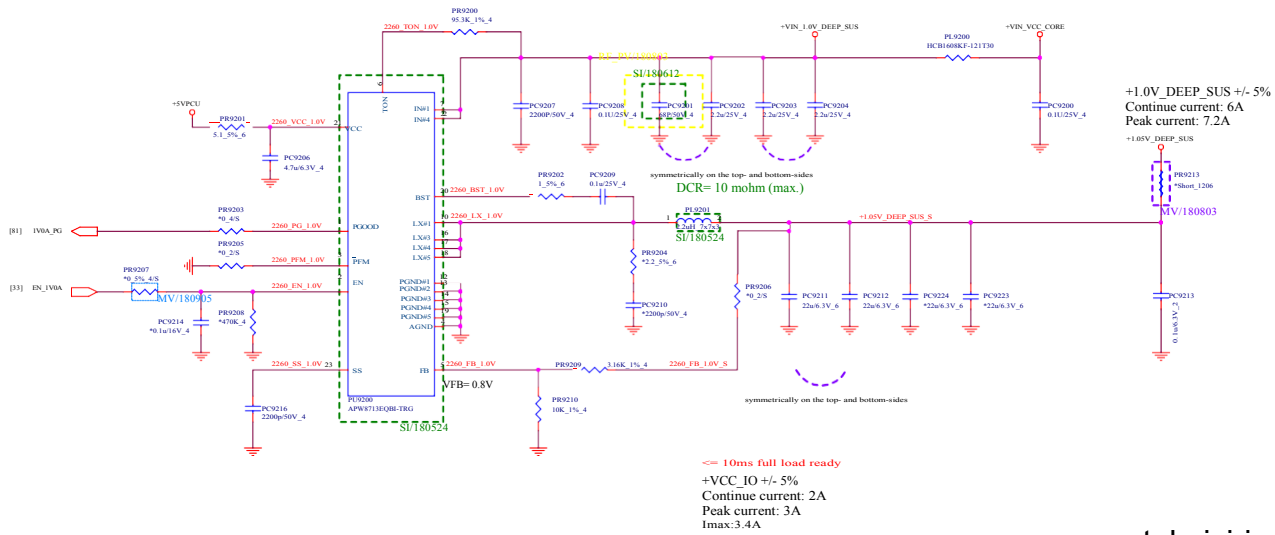
[11,33,41,73,75,81,86,87,93] +3V_ALW



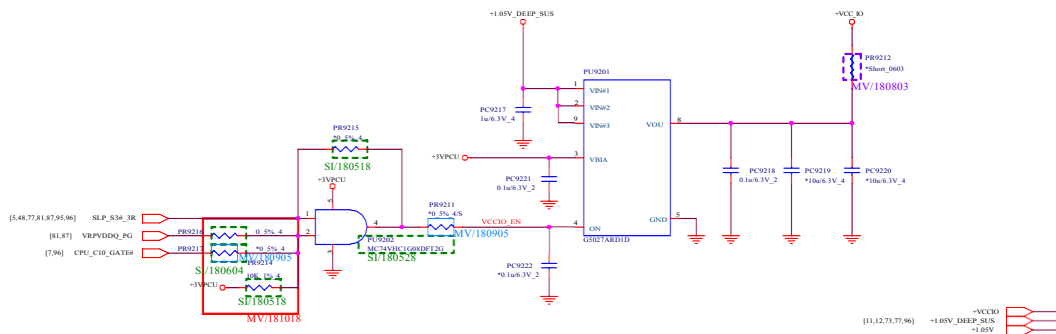





Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k



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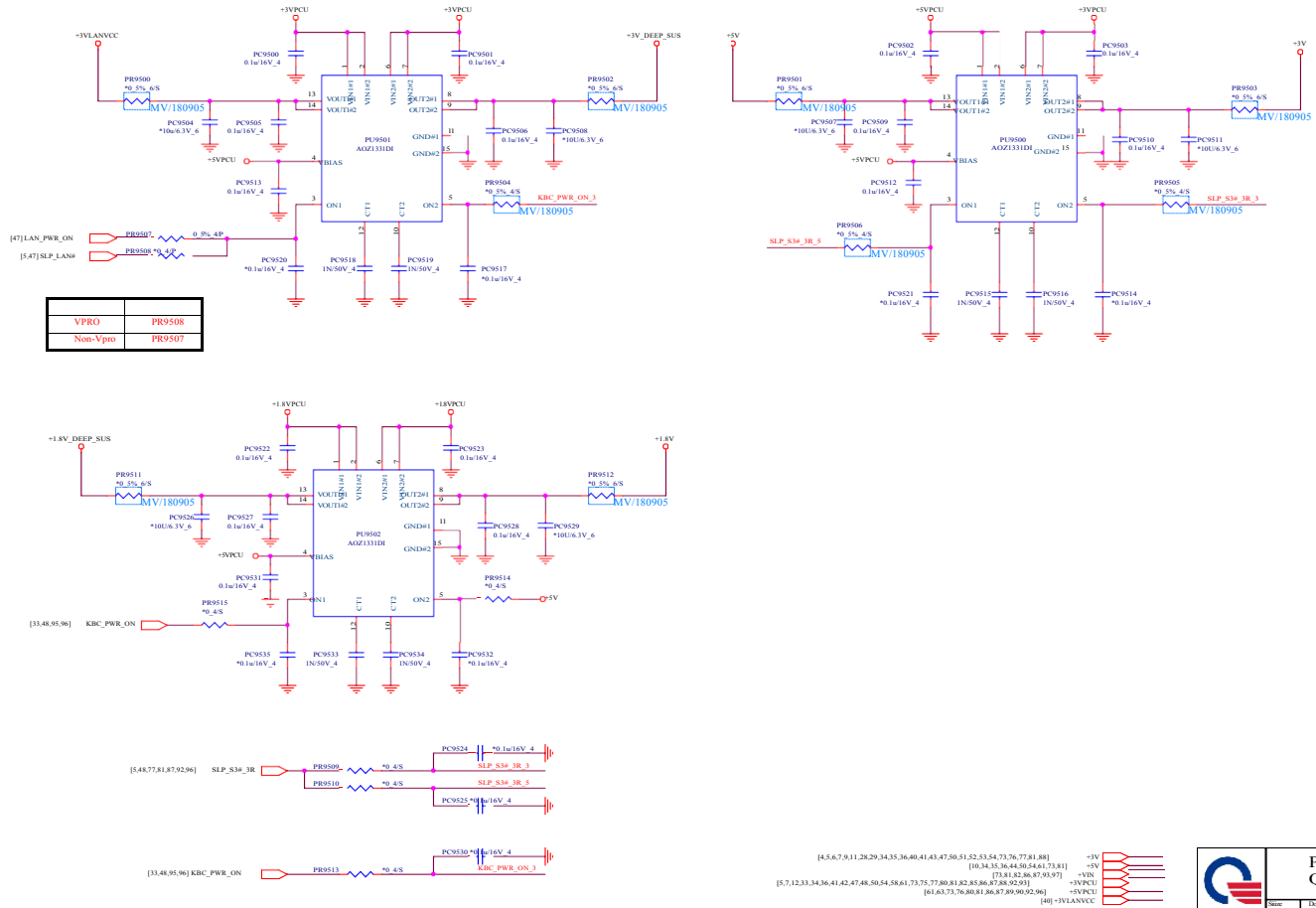




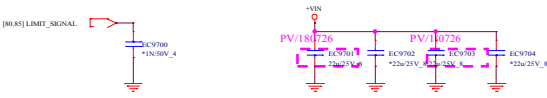
PROJECT : 400 SERIES

Quanta Computer Inc.

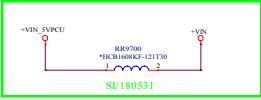
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Reserve for EMI & ISEN test





RF Cap





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Quanta Computer Inc.


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Quanta Computer Inc.

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	Quanta Computer Inc.		
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